CLAIM AMENDMENTS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) In a wireless receiver, a circuit for receiving an input signal from a transmitter, the input signal including a preamble portion, a unique word portion and a data portion, the circuit comprising:
   a. a preamble detector configured to receive the input signal and to provide a preamble signal where the preamble signal is active during the preamble portion of the input signal and inactive during all portions of the input signal other than the preamble portion;
   b. a DC level set circuit configured to receive the preamble signal, the input signal including the preamble portion, the unique word portion and the data portion and to receive a control signal and to provide a level set signal; ~~and~~
   c. a data slicer circuit coupled with the DC level set circuit to receive the level set signal and to provide the output signal; and
   d. a delay line for receiving the input signal and for providing a delay signal to the DC level set circuit.

2. (currently amended) The circuit of Claim 1 wherein the preamble detector comprises:
   a. an AC coupling for removing a direct current offset from the input signal;
   b. a first comparator for recovering a digital output from the AC coupling;
   c. ~~a four bit delay line for detecting and for holding the preamble portion of the input signal;~~
   ~~d.~~ a lower block coupled with both the four bit delay line and the first comparator for providing the preamble signal when the four bit delay line detects the preamble portion of the input signal; and
   [[e]]d. a delay element for receiving the input signal and for providing a delay signal to the DC level set circuit, wherein the delay line is a four bit delay line.

3. (previously presented) The preamble detector of Claim 2 wherein the lower block outputs an active output to the DC level set circuit.

4. (original) The preamble detector of Claim 2 wherein the delay element delays the input signal one-twelfth of one bit.

5. (original) The circuit of Claim 1 wherein the DC level setting circuit comprises:
   a. a functional AND gate for receiving the preamble signal and the control signal and outputting a switch signal when both the control signal and the preamble signals are active;
   b. an integrating capacitor coupled in parallel with a current source for charging or discharging the integrating capacitor;
   c. a second comparator for comparing the input signal to an output from the integrating capacitor and for outputting a charge signal;
   d. a first summer for adding the delay signal from the preamble detector to the charge signal of the second comparator;
   e. a switch for providing an electrical connection from the first summer to the current source; and
   f. a second summer for adding the output of the integrating capacitor with the input signal and for outputting the level set signal to the data slicer.

6. (original) The DC level setting circuit of Claim 5 wherein when the charge of the integrating capacitor is less than the input signal, the charge signal causes the current source to charge the integrating capacitor.

7. (original) The DC level setting circuit of Claim 5 wherein when the charge of the integrating capacitor is more than the input signal, the charge signal causes the current source to discharge the integrating capacitor.

8. (original) The DC level setting circuit of Claim 5 wherein the switch closes when the functional AND gate outputs the switch signal, and opens when the switch signal is not outputted by the functional AND gate.

9. (original) The circuit of Claim 1 wherein the data slicer circuit comprises:
   a. an analog comparator;
   b. a one bit resolution delay line; and
   c. a third summer.

10. (original) The data slicer circuit of Claim 9 wherein a third summer is configured to receive the level set signal from the DC level set circuit.

11. (original) The data slicer circuit of Claim 9 wherein the third summer subtracts a scaled feedback signal from the level set signal.

12. (original) The data slicer circuit of Claim 9 wherein the analog comparator is configured to receive an output of the third summer and to produce the output signal.

13. (original) The data slicer circuit of Claim 9 wherein the one bit resolution delay line is configured to receive the output signal as a feedback signal.

14. (original) The data slicer circuit of Claim 9 wherein the one bit resolution delay line outputs the scaled feedback signal.

15. (currently amended) A method of receiving an input signal and a control signal and providing an output signal, the input signal including a preamble portion, a unique word portion and a data portion, the method comprising the steps of:

a. receiving the input signal with a preamble detector;
b. providing a preamble signal where the preamble signal is active during the preamble portion of the input signal and inactive during all portions of the input signal other than the preamble portion;
c. receiving the preamble signal from the preamble detector, the input signal and the control signal with a DC level set circuit;
d. providing a level set signal with the DC level set circuit;
e. receiving the level set signal from the DC level set circuit with a data slicer circuit; and
f. providing the output signal with the data slicer circuit,

wherein the preamble detector provides the preamble signal to the DC level setting circuit when a delay line detects the preamble portion of the input signal.

16. (currently amended) The method of Claim 15 wherein the delay line is~~preamble detector provides the preamble signal to the DC level setting circuit when~~ a four bit delay line ~~detects the preamble portion of the input signal~~.

17. (original) The method of Claim 15 wherein the data slicer circuit provides the output signal by:

$$d_k = x_k - 0.17d_{k-m}$$

where d_k is the current output, x_k is the current input and d_{k-m} is the previous bit decision.

18. (currently amended) A circuit for receiving an input signal and a control signal and providing an output signal, the input signal including a preamble portion, a unique word portion and a data portion, the circuit comprising:

a. means for receiving the input signal with a preamble detector;

b. means for providing a preamble signal where the preamble signal is active during the preamble portion of the input signal and inactive during all portions of the input signal other than the preamble portion;

c. means for receiving the preamble signal from the preamble detector, the input signal and the control signal with a DC level set circuit;

d. means for providing a level set signal with the DC level set circuit;

e. means for receiving the level set signal from the DC level set circuit with a data slicer circuit; ~~and~~

f. means for providing the output signal with the data slicer circuit; and

g. means for detecting and holding the preamble portion of the input with a delay line.

19. (currently amended) The circuit of Claim 18 wherein the preamble detector comprises:

a. an AC coupling for removing a direct current offset from the input signal;

b. a first comparator for recovering a digital output from the AC coupling;

c. ~~a four bit delay line for detecting and for holding the preamble portion of the input signal;~~

~~d.~~ a lower block coupled with both the four bit delay line and the first comparator for providing the preamble signal when the four bit delay line detects the preamble portion of the input signal; and

[[e]]d. a delay element for receiving the input signal and for providing a delay signal output to the DC level set circuit, wherein the delay line is a four bit delay line.

20. (original) The preamble detector of Claim 19 wherein the lower block outputs the active output to the DC level set circuit.

21. (original) The preamble detector of Claim 19 wherein the delay element delays the input signal one-twelfth of one bit.

22. (original) The circuit of Claim 18 wherein the DC level setting circuit comprises:
   a. a functional AND gate for receiving the preamble signal and the control signal and outputting a switch signal when both the control signal and the preamble signals are active;
   b. an integrating capacitor coupled in parallel with a current source for charging or discharging the integrating capacitor;
   c. a second comparator for comparing the input signal to an output from the integrating capacitor and for outputting a charge signal;
   d. a first summer for adding the delay signal from the preamble detector to the charge signal of the second comparator;
   e. a switch for providing an electrical connection from the first summer to the current source; and
   f. a second summer for adding the output of the integrating capacitor with the input signal and for outputting the level set signal to the data slicer.

23. (original) The DC level setting circuit of Claim 22 wherein when the charge of the integrating capacitor is less than the input signal, the charge signal causes the current source to charge the integrating capacitor.

24. (original) The DC level setting circuit of Claim 22 wherein when the charge of the integrating capacitor is more than the input signal, the charge signal causes the current source to discharge the integrating capacitor.

25. (original) The DC level setting circuit of Claim 22 wherein the switch closes when the functional AND gate outputs the switch signal, and opens when the switch signal is not outputted by the functional AND gate.

26. (original) The circuit of Claim 18 wherein the data slicer circuit comprises:
    a. an analog comparator;
    b. a one bit resolution delay line; and
    c. a third summer.

27. (original) The data slicer circuit of Claim 26 wherein a third summer is configured to receive the level set signal from the DC level set circuit.

28. (original) The data slicer circuit of Claim 26 wherein the third summer subtracts a scaled feedback signal from the level set signal.

29. (original) The data slicer circuit of Claim 26 wherein the analog comparator is configured to receive an output of the third summer and to produce the output signal.

30. (original) The data slicer circuit of Claim 26 wherein the one bit resolution delay line is configured to receive the output signal as a feedback signal.

31. (original) The data slicer circuit of Claim 26 wherein the one bit resolution delay line outputs the scaled feedback signal.